



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,157	02/02/2004	Sadayuki Morita	501.43367X00	6025

20457 7590 08/24/2005

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER

SOFOCLEOUS, ALEXANDER

ART UNIT PAPER NUMBER

2824

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/768,157

Applicant(s)

MORITA ET AL.

Examiner

Alexander Sofocleous

Art Unit

2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02/02/2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 February 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date (1) 2/2/2005.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☒ Other: Search History.

DETAILED ACTION

1. This action is responsive to the following communications: the Application and Preliminary Amendment filed on February 2, 2004, the Foreign Priority filed on February 2, 2004, and the Information Disclosure Statement filed on February 2, 2004.

2. Claims 1-12 are pending in the case. Claims 1 and 7 are independent claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received in Application.

Title

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: microprocessor coupled memory with level-shifting buffers.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

On Fig. 1, the components labeled 11-4, 103-4, 21-4, and 206-4 do not exist. Examiner assumes that the fore-mentioned labels are similar to the generic blocks 11-n, 103-n, 21-n, and 206-n as representation for the detailed blocks 11-3, 103-3, 21-3, and 206-3, respectively; however, it is suggested that

Art Unit: 2824

generic blocks for 11-4, 103-4, 21-4, and 206-4 be inserted into Figure 1, in similar form as 11-n, 103-n, 21-n, and 206-n.

On Fig. 2, which Fig. 8 depends, the bonding pad 30-1, 30-2, and 30-3 do not exist (See Page 20 line 22). It is suggested that 30-1 and 30-2 on Fig. 8 and Fig. 1 be labeled 31-1 and 31-2, respectively, to be consistent with Fig. 2. It is also suggested that a bonding pad, 31-3, be added to Fig. 2. Also, the specification should be corrected accordingly; e.g., on page 8 line 22, "...bonding pads 30-1 and 30-2..." should be corrected to read, "... bonding pads 31-1 and 31-2..." Several other areas in the specification need to be corrected as well.

On Fig. 7, which depends on Fig. 6, the bonding pad 30-1 should be relabeled 31-1 to conform to the labeling strategy of Fig. 6. Also, the specification needs to be corrected, in a fashion described above, accordingly.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Art Unit: 2824

Specification

6. The disclosure is objected to because of the following informalities: Several locations make use of the word "negative" to denote the negation of a logic signal. The examiner believes that "NOT" is a more appropriate word, as "NOT" is well known in this art and other fields relating to binary logic to represent the negation of a logic signal. For example, on page 9 line 24, the specification states, "...includes a NAND gate 81 that attains the negative AND state..." Such change would read as, "...includes a NAND gate 81 that attains the NOT AND state..." Several locations of such minor informalities are, but, not limited to: Page 9 line 14, Page 9 line 25, Page 10 line 4, Page 13 line 3, Page 13 line 7, and Page 13 line 18.

Also, on Page 16 line 4, the specification refers to "step-down circuit 9." Examiner assumes that applicant means "step-down circuit 90." It is suggested that "9" be corrected to "90."

Appropriate correction is required.

Claim Objections

7. Claim 12 is objected to because of the following informalities: it is suggested that "any of" in line 1 be changed to "any one of" for clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

Art Unit: 2824

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujita U.S. Patent No. 5,359,569.

Regarding independent claim 1, Fig. 1 of Fujita shows a semiconductor device comprising a data control circuit (Fig. 1 [4]) coupled with a memory (Fig. 1 [2]). The memory is capable of being accessed by the microprocessor (Fig. 5 [32]) inside of the data control circuit.

The data control circuit (Fig. 5 [4]) contains a buffer (Fig. 5 [46]) for the microprocessor, or system side. The data control circuit is supplied the power supply voltage (Fig. 1 [7]). Although no specific voltage line is shown for the buffer, electronic buffers inherently operate with an input voltage. The data line from the buffer (Fig. 5 [DATA]) allows for the exchange of signals with the outside.

The internal power supply circuit (Fig. 1 [power supply circuit]) takes a voltage from the power source (Fig. 1 [power source]), which is a reference voltage. The power supply unit (Fig. 1 [7]) generates an output power supply voltage that is inputted to diodes. The output lines of the internal power supply circuit are the same lines as the output of the power supply unit; i.e., the internal power supply circuit voltage is substantially equal to power supply voltage.

The figures show buffers (Fig. 5 [47, 48]) for the memory side. The data control circuit is supplied the power supply voltage from the power supply unit. Although no specific voltage line is shown for the buffer, the data control circuit is

Art Unit: 2824

supplied a voltage to power the components of the data control circuit and buffers must be supplied a voltage in order to operate. The buffer on the memory side is connected to the buffer on the microprocessor side inside the data control circuit; thus, the memory side exchanges data with the system side through the fore-mentioned buffers and will only be capable of exchanging data if the buffers are supplied the power supply voltage.

Regarding dependent claim 2 and in addition to the claims covered above, Fujita shows in Fig. 1 that the memory takes voltage from the power supply unit via some terminal. The memory block is a replaceable component in this patent; thus, having an external voltage terminal is an inherent property of this semiconductor memory.

Regarding dependent claim 3 and in addition to the claims covered above, Fujita shows in Fig. 5 a microprocessor inside a data control circuit. The data control circuit that takes the power supply voltage in order to supply the components of the data control circuit with voltage. Microprocessors are known in the art to be comprised of internal circuits that are put in operation when supplied with a voltage.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujita U.S. Patent No. 5,359,569 in view of Kobayashi U.S. Patent Application Publication No. US2002/0064077A1 as supported by Ovens U.S. Patent Application No. US2002/0024374A1.

Regarding dependent claim 4, Fujita sets forth all of the claim elements, as disclosed above, except for the differential circuit component of the internal power supply. Fujita is also silent with respect to a voltage output circuit that determines the level of voltage on basis of a comparison result in the differential circuit. Ovens teaches in the disclosure that memory and microprocessors are integrated circuits, ICs, and that ICs are semiconductors (paragraph 0002). Kobayashi teaches a semiconductor device comprising a differential circuit component of the internal power supply and a voltage output circuit that determines a level of voltage on basis of a comparison result in the differential circuit; but, does not suggest coupling a microprocessor with a memory. Fujita teaches coupling a microprocessor with a memory.

Ovens' description of microprocessors and memories being semiconductors is applicable to Kobayashi semiconductor as being a microprocessor or a memory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the internal power supply circuits to generate internal voltages based off of an

Art Unit: 2824

externally supplied voltage in order to ensure reliability inside of the semiconductor device (Kobayashi paragraph [0006]).

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits.

Regarding dependent claim 5, Fujita in view of Kobayashi as supported by Owens shows coupling memory hosting internal power supply circuitry with a microprocessor hosting internal power supply circuitry. Fujita sets forth all of the claim elements, as disclosed above, except for internal memory circuits that are put into operation when supplied a higher voltage than the internal power supply voltage, and an input/output buffer that is capable of shifting an internal power supply voltage into the signal level of a second internal power supply voltage by a level-shifting circuit. Kobayashi shows internal memory circuitry (Fig. 1 [38]) that is put into operation when supplied with a higher voltage than the internal power supply voltage and also shows input/output buffers (Fig. 1 [20 and 34]) comprising level-shifting circuitry, i.e., a boosted power supply circuit (Fig. 1 [36]), and a step-down circuit (Fig. 1 [38]). Additionally, circuitry, internal to a memory, that is put into operation by being supplied a voltage is an inherent property of semiconductor memory. Kobayashi further shows a semiconductor device, or memory, that comprises a boosted power supply circuit (Fig. 1 [36]) capable of boosting a voltage to a reference voltage (Fig. 1 [Ext. Vcc]). The boosted voltage

Art Unit: 2824

is used to generate an internal voltage (Fig. 1 [Int. Vcc]) to provide power to internal circuitry (paragraph [0083]), i.e., input/output buffers, memory, etc.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the memory internal power supply circuits to generate internal voltages based off of an externally supplied voltage in order to ensure reliability inside of the semiconductor device (Kobayashi paragraph [0006]).

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits.

Regarding dependent claim 6, Fujita in view of Kobayashi as supported by Owens shows coupling memory hosting internal power supply circuitry with a microprocessor hosting internal power supply circuitry. Fujita sets forth all of the claim elements, as disclosed above, except for a step-down circuit for the memory that generates an internal voltage, lower than the internal power supply voltage, that is sent to a voltage boosting circuit used by the input/output buffers to match the voltage of the internal power supply voltage. Kobayashi shows a semiconductor device, or a memory, comprising a step-down circuit (Fig. 1 [38]) that lowers an internal power supply voltage (Fig. 2 [Vref]). Circuitry, internal to a

Art Unit: 2824

memory, that is put into operation by being supplied a voltage is an inherent property of semiconductor memory. Kobayashi further shows a voltage boosting circuit (Fig. 1 [36]) that is capable of internally outputting a voltage (Fig. 1 [Vpp]) that matches the level of a reference voltage (Fig. 1 [Ext. Vcc]) in order to be used to generate another internal voltage (Fig. 1 [Int. Vcc]) to provide power to internal circuitry (paragraph [0083]), i.e., input/output buffers, memory, etc.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the internal power supply circuits to generate internal voltages based off of an externally supplied voltage in order to ensure reliability inside of the semiconductor device (Kobayashi paragraph [0006]).

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits. Ovens further shows that level-shifting significantly reduces setup and clock-to-Q times and allows for higher speed industry specifications to be met (abstract).

Regarding independent claim 7, Fujita shows a microprocessor coupled with a memory and an input/output buffer for the memory side that is capable of exchanging data with the input/output buffer for the system side when supplied

Art Unit: 2824

an internal power supply voltage; but, is silent with respect to the microprocessor comprising an internal core power supply circuit and a input/output buffer for the system that is capable of exchanging data with the input/output buffer when supplied the internal core voltage. Also, Fujita is silent with respect to the memory comprising an internal power supply that takes the internal core power supply voltage as a reference voltage and generates an internal voltage that is substantially equal to the internal power supply voltage. Owens teaches in the disclosure that memory and microprocessors are integrated circuits, ICs, and that ICs are semiconductors (paragraph 0002). Owens' description of microprocessors and memories being semiconductors is applicable to Kobayashi semiconductor as being a microprocessor or a memory. Kobayashi shows a semiconductor device, or a microprocessor, comprising internal power supply circuitry (Fig. 1 [36 and 38]), with a step-down circuit(Fig. 1 [38]), that generates an internal voltage (Fig. 1 [Int. Vcc]) by stepping down a reference voltage (Fig. 2 [Vref]). Kobayashi shows input/output buffers (Fig. 1 [20 and 34]) that are powered by the generated internal voltage (Fig. 1 [Int. Vcc]) (paragraph 0083). Kobayashi further shows a semiconductor device, or a memory, that comprises internal power supply circuitry (Fig. 1 [36 and 38]) that is capable of generating an internal voltage (Fig. 1 [Int. Vcc]) from a reference voltage (Fig. 2 [Vref]). Kobayashi also shows input/output buffers for that are put into operation by being supplied an internal voltage.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a

Art Unit: 2824

Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the internal power supply circuits to generate internal voltages based off of an externally supplied voltage in order to ensure reliability inside of the semiconductor device (Kobayashi paragraph [0006]).

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits.

Regarding independent claim 8, Fujita in view of Kobayashi as supported by Owens sets forth all of the above disclosed claim elements. Fujita shows memories (Fig. 1 [2 and 4]) that is supplied voltage from the power supply unit. The memory block is a replaceable component in this patent; thus, having an external voltage terminal is an inherent property of this semiconductor memory.

Regarding independent claim 9, Fujita in view of Kobayashi as supported by Owens sets forth all of the above disclosed claim elements. Fujita shows a microprocessor (Fig. 5 [43]) that is supplied voltage from the power supply unit. The microprocessor block is a replaceable component in this patent; and, it is well known in the art that circuits internal to the microprocessor that are put into operation by a power supply voltage is an inherent property of a microprocessor.

Regarding independent claim 10, Fujita in view of Kobayashi as supported by Owens sets forth all of the above disclosed claim elements. Fujita does not show an internal power supply circuit that comprises a differential circuit and a voltage output circuit. Kobayashi shows a voltage converting unit (Fig. 2 [54] comprising a differential circuit (Fig. 2 [56]) that outputs a voltage (Fig. 2 [Int. Vcc]) on basis of comparison between a reference voltage (Fig. 2 [Vref]) and the internal voltage (Fig. 2 [Int. Vcc]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the internal power supply circuits to generate internal voltages based off of an externally supplied voltage in order to ensure reliability inside of the semiconductor device (Kobayashi paragraph [0006]).

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits.

Regarding independent claim 11, Fujita in view of Kobayashi as supported by Owens sets forth all of the above disclosed claim elements. It is well known in the art of microprocessors that internal clock drivers that are

Art Unit: 2824

capable of outputting a clock signals are inherent to semiconductor microprocessors. Furthermore,

Regarding independent claim 12, Fujita in view of Kobayashi as supported by Owens sets forth all of the above disclosed claim elements. Fujita further shows packaging the microprocessor and memory. The memory (Fig. 1 [2 and 4]) and microprocessor (Fig. 5 [43]) blocks are separate units packaged in the same block (Fig. 1 [1]). Fujita shows a memory block; but, is silent with respect to the memory being synchronous. Kobayashi shows a semiconductor with clock driving circuitry (Fig. 1 [22]) with accompanying logic circuitry (Fig. 1 [18]) that generates a clock control from input strobe signals (Fig. 1 [Ext./RAS and Ext./CAS]) (paragraph 0080).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teachings of Fujita to Kobayashi such that a Kobayashi representation of a memory replaces the Fujita memory (Fig. 1 [2,5]) and a Kobayashi representation of a microprocessor replaces the Fujita microprocessor (Fig. 5 [43]) for the purpose of allowing the memory and microprocessor to host clock driving circuits in order to synchronize data transmissions.

Further motive to perform the above stated modifications are evidenced by the fact that both Fujita and Kobayashi are from the same field of endeavor such as being semiconductor devices with memories, buffers, and power supply circuits.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kang (U.S. Patent Application 2004/01385A1), and Park et al. (U.S. Patent Application 2002/0181310A1). Kang shows a plural arrangement of semiconductor memories with power circuits therein and connected output buffers. Park et al. shows that most semiconductor memories include internal voltage generators. Also, Park shows an internal voltage generator for memory that can uniformly supply a predetermined amount of electrical charge and can generate a stable internal voltage from an external reference voltage.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

A shortened statutory period for response to this action is set to expire three months and zero days from the date of this letter. Failure to respond within the period for response will cause this application to become abandoned (see MPEP 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax

Art Unit: 2824

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGS

A handwritten signature in black ink, appearing to read 'Richard Elms', with a date stamp '8/22/05' written next to it.

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800